REVISION HISTORY

DEVICE ORDER INFORMATION

25'(5$%/('(9,&(	3$&.$*,1* 7<3(	67$1'$5' 3$&. 47<	3$&.$*(0$5.,1*	3,16	3$&.$*('(6&5,37,21

THERMAL INFORMATION

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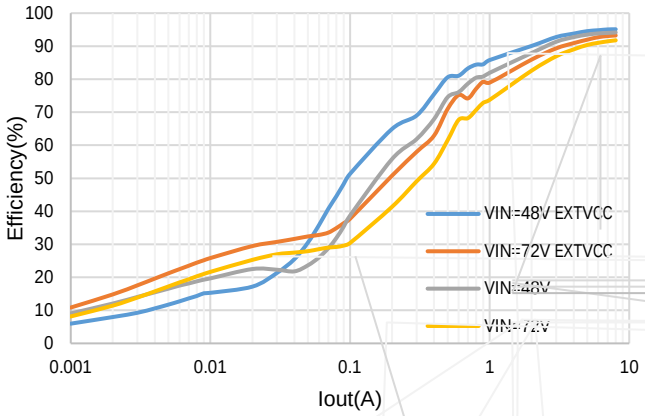
6<0%2	3$5$0(7(5	7(67 &21',7,21	0,1 7<3 0$;	81,7

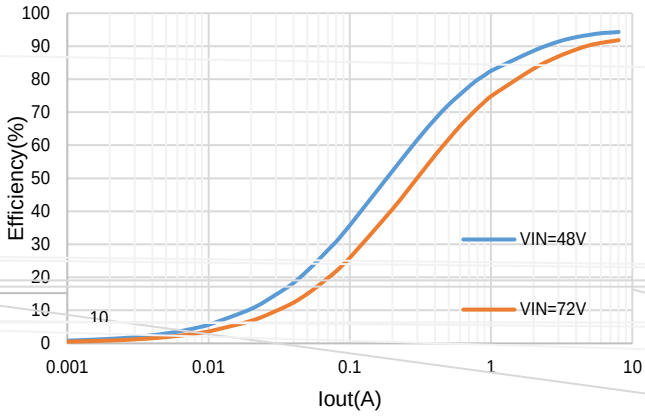
6RIWWDUW DQG 9ROWDJH 7UDFNLQJ

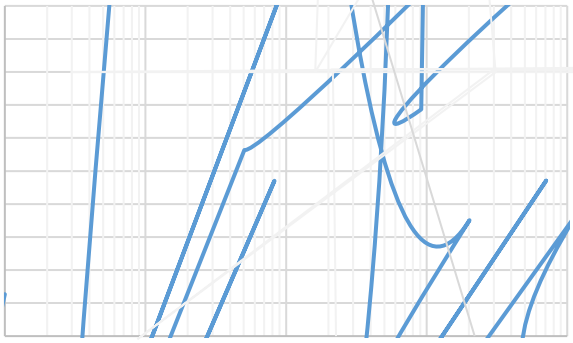
3RZHU *RRG ,QGLFDWRU

6<0%2	3$5$0(7(5	7(67 &21',7,21	0,1 7<3 0$;	81,7

TYPICAL CHARACTERISTICS

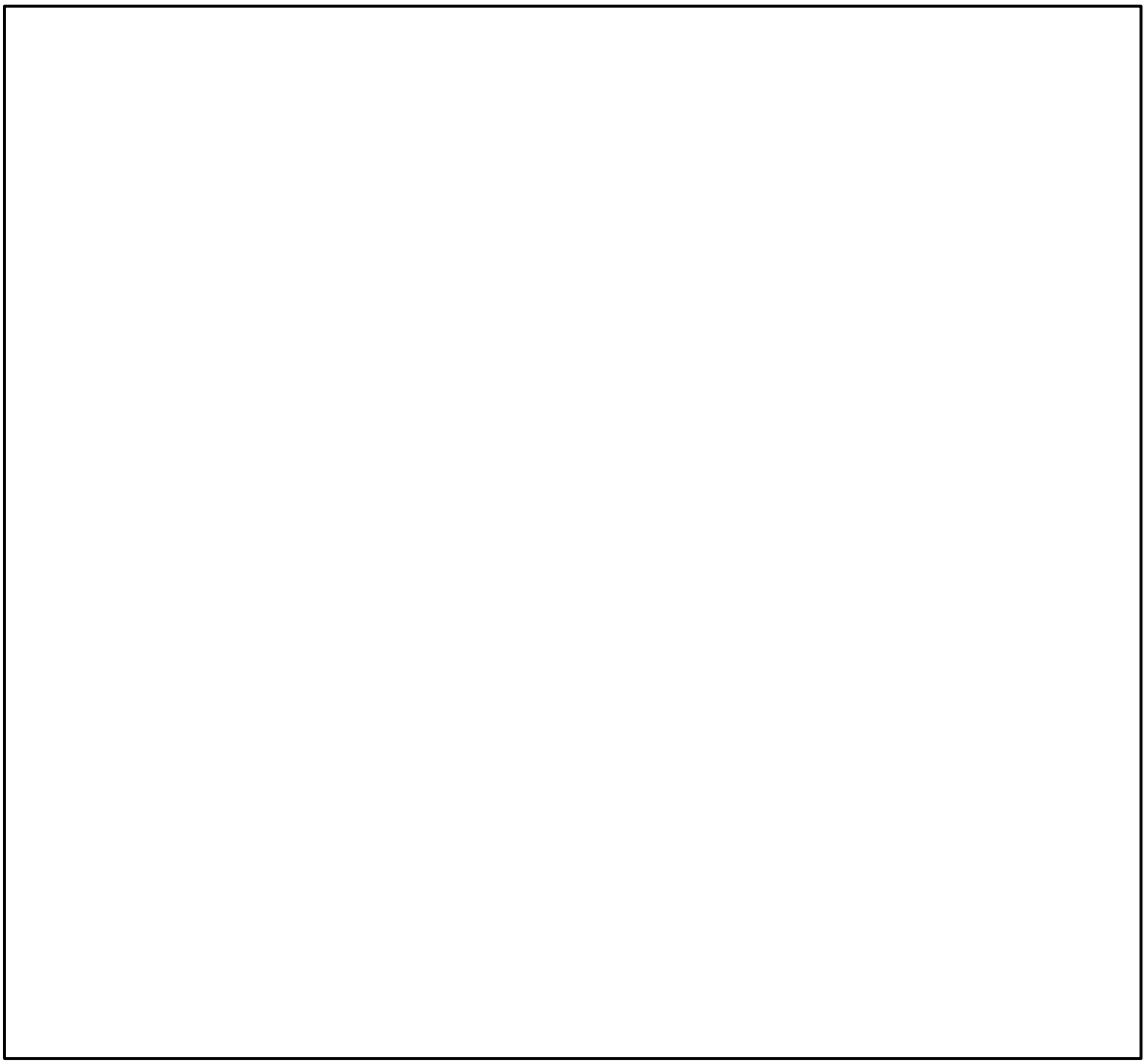






TYPICAL CHARACTERISTICS

FUNCTIONAL BLOCK DIAGRAM



SW

OPERATION

2 Y H U Y L H Z

The VCC regulator output has a current limit of 40 mA (minimum). At power up, when the VCC voltage exceeds its rising UVLO threshold of 4.5 V the output is enabled if EN is above 1.2V, and the soft-start sequence begins. The output remains active until the VCC voltage falls below its falling UVLO threshold of typical 4.3 V or if EN goes to a standby or shutdown state.

There are two ways powering the VCC pin with the external source helping to increase overall efficiency and decrease internal self-heating due to power dissipated in the LDO. One is to connect a bias supply rail (up to 13V) to VCC using a diode. Or powering the EXTVCC pin with an external power source or from output voltage directly which is very convenient for customer especially when output voltage is setup at 5.5V as shown in Figure 20. If the EXTVCC pin is tied to an external source larger than 4.7V (max 5.5V), then the internal VCC LDO is shut down and an internal switch shorts the EXTVCC pin to the VCC pin. This external power source could be the output of the buck switching converter itself if the output is programmed to higher than 4.7V (max 5.5V).

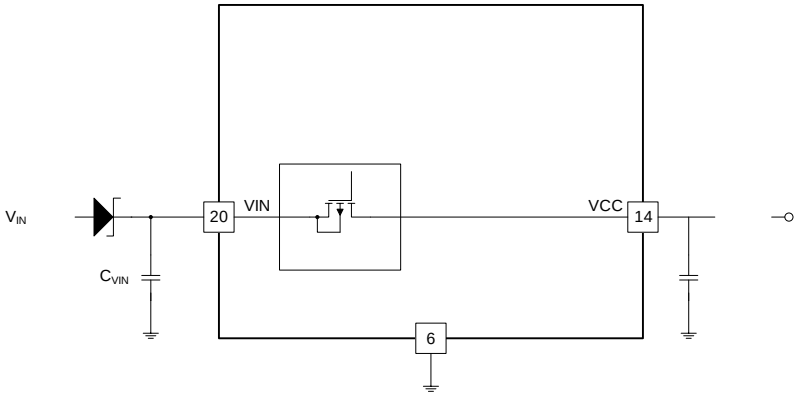


Figure 20. VCC Bias Supply Connecting EXTVCC Auxiliary Supply

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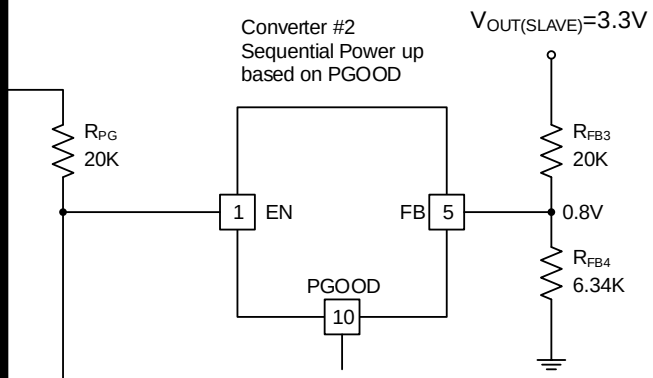
The SCT82A31 can be shut down using the EN pin. Pulling this pin below 1.2V prevents the controller from switching, and less than 0.41V disables most of the internal bias circuitry, including the VCC regulator. The shutdown IQ is about 7.2



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'HYLFH)XQFWLRQDO 0RGHV

Shutdown Mode

The EN pin provides ON / OFF control for the SCT82A31. When the EN voltage is below 0.38V typical, the device is in shutdown mode. Both the internal bias supply LDO and the switching regulator are off. The quiescent current in shutdown mode drops to 7.2 SCT82A31 also includes under voltage protection of the internal bias LDO. If the internal bias supply voltage is below its UVLO threshold level, the switching regulator remains off.

Standby Mode

The internal bias supply LDO has a lower enable threshold than the switching regulator. When the EN voltage exceeds 0.41 V typical and is below the precision enable threshold 1.2 V typically, the internal LDO is on and regulating. Switching action and output voltage regulation are disabled in standby mode.

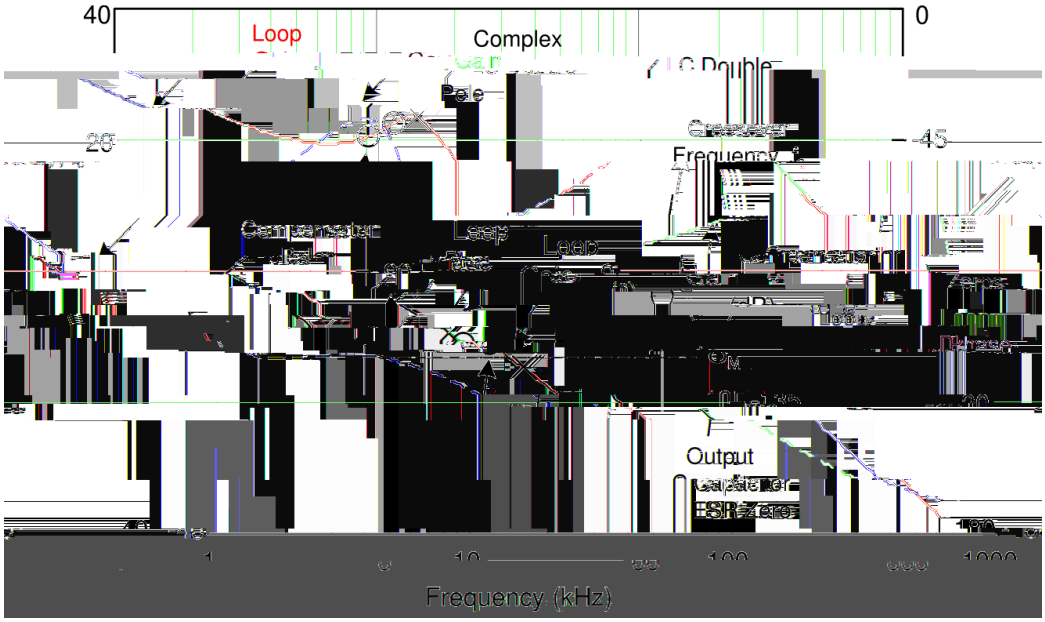
Active Mode

The SCT82A31 is in active mode when the VCC voltage is above its rising UVLO threshold of 5 V and the EN voltage is above the precision EN threshold of 1.2 V. The simplest way to enable the SCT

Duty-cycle-to-output transfer function	$G_{vd}(s) = \frac{V_o(s)}{d(s)} \cdot V_{IN} \cdot \frac{1 + \frac{s}{\omega_{ESR}}}{1 + \frac{s}{Q_o \omega_o} + \frac{s^2}{\omega_o^2}}$
Compensator transfer function	$G_C(s) = \frac{V_{comp}(s)}{V_o(s)} = \frac{1}{R_{FB} C_C s} \cdot \frac{\left(1 + \frac{s}{\omega_{z1}}\right)\left(1 + \frac{s}{\omega_{z2}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)}$
Modulator transfer function	$F_m = \frac{d(s)}{V_{comp}(s)} = \frac{1}{V_{ramp}}$

The compensation network typically employed with voltage-mode control is a Type-III circuit with three poles and two zeros. One compensator pole is located at the origin to realize high DC gain. The normal compensation strategy uses two compensator zeros to counteract the LC double pole, one compensator pole located to nullify the output capacitor ESR zero, with the remaining compensator pole located at one-half switching frequency to attenuate high

$\sqrt{\quad}$	$_{ESR}$ $\overline{R_{ESR} \quad C_{OUT}}$	$_{p}$ $\overline{R_C \quad C_C}$	
		$_{p}$ $\overline{R_C \quad C_C}$	$_{z}$ $\overline{R_{FB} \quad R_C \quad C_C}$



$$T_V \; s \quad \frac{V_{IN}}{V_{ramp}} \; \frac{}{s \; R_{FB} \quad C_C} \; \overline{K}$$

$$_{c} \qquad f_C \quad \frac{}{R_{FB} \quad C_C} \; \frac{V_{IN}}{V_{ramp}} \; \overline{K}$$

&] . &R &] &R &S &6:

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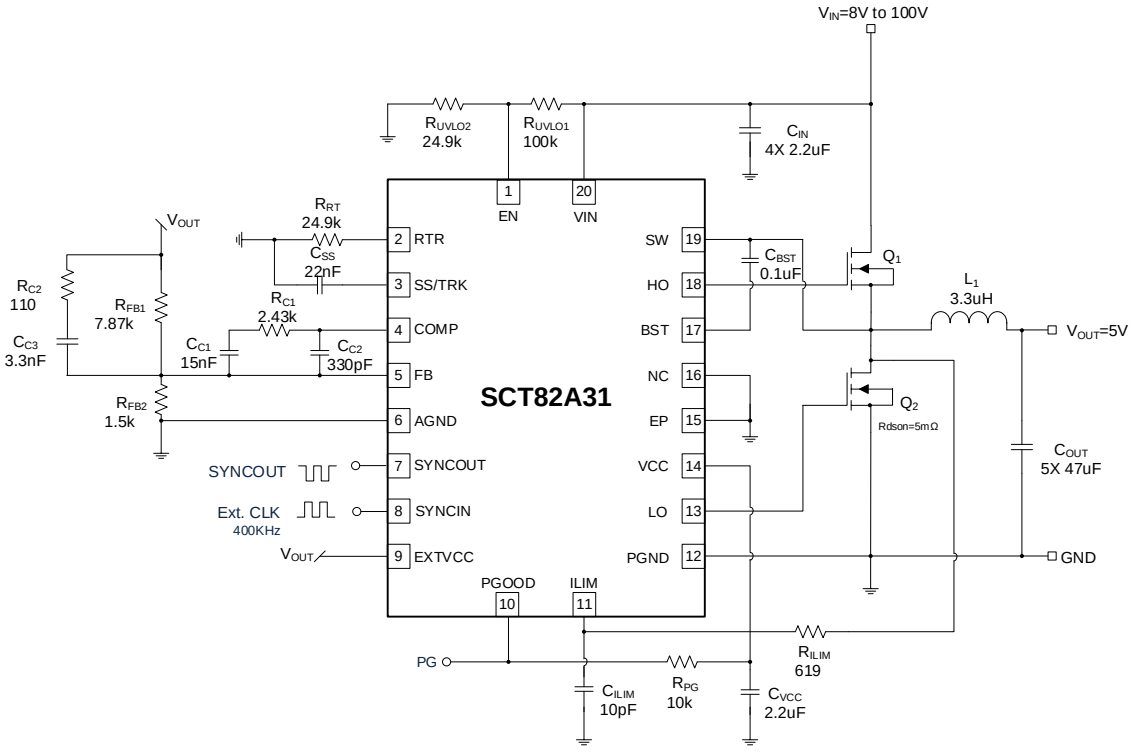
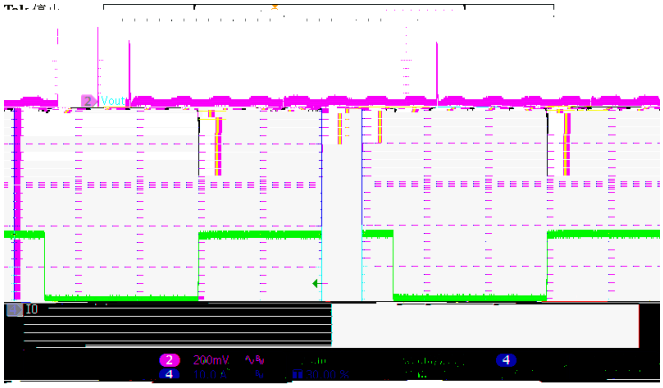


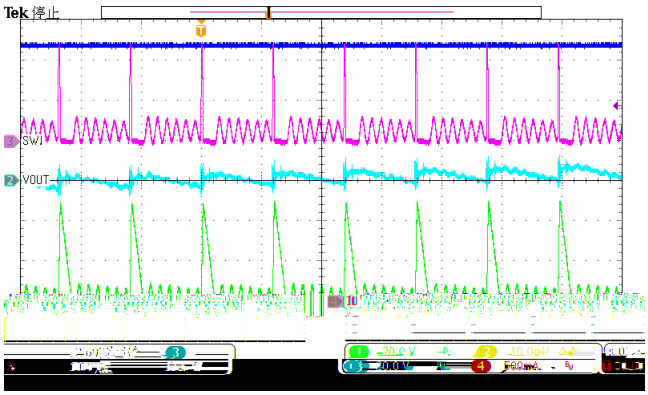
)LJXUH $SSOLFDWLRQ 69FKWHPDWLF% XFN 5HJXODWRU DW N+]

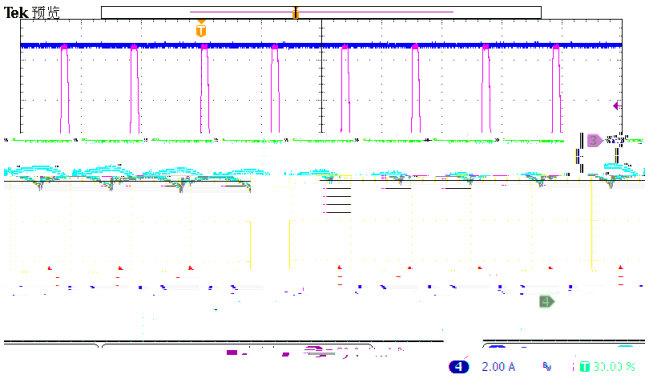
'HVLJQ3URFHGXUHV

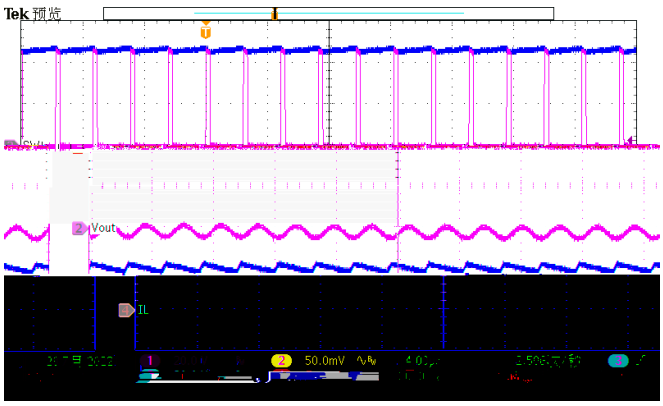
$SSOLFDWLRQ :DYHIRUPV

$ S S O L F D W L R Q : ÐRY QH WRLUQPXVH G









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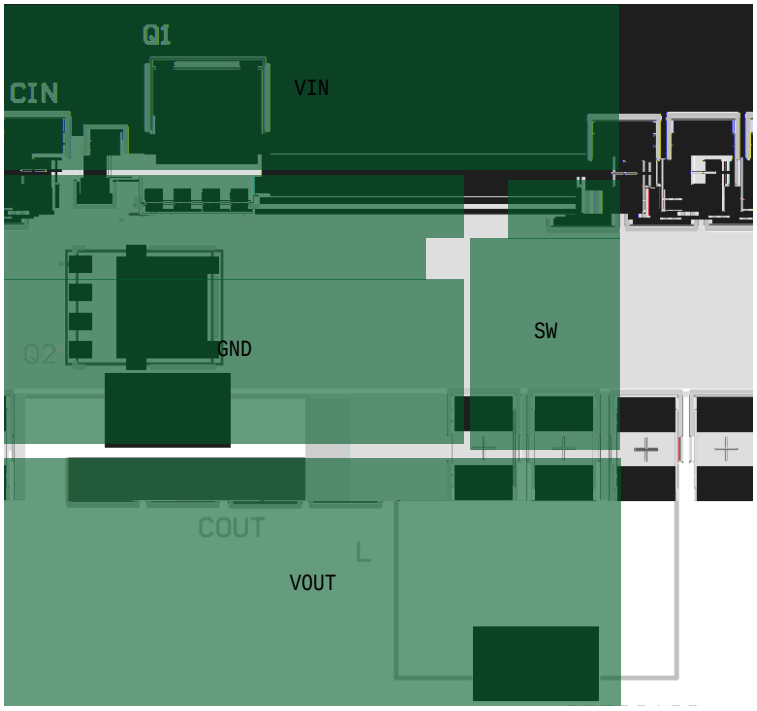
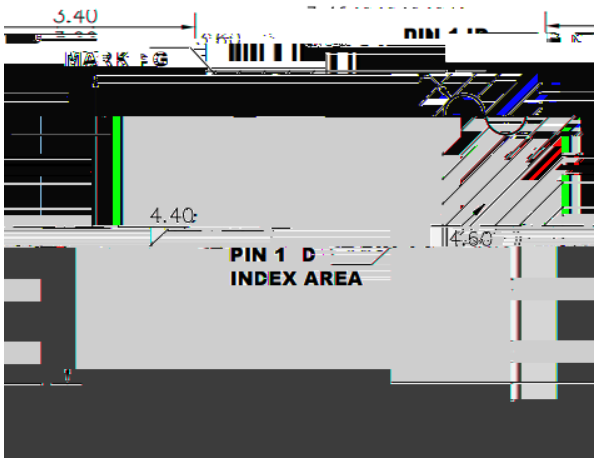
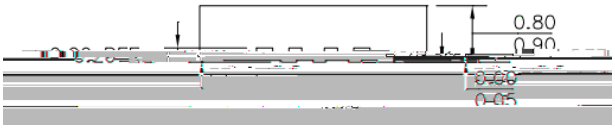
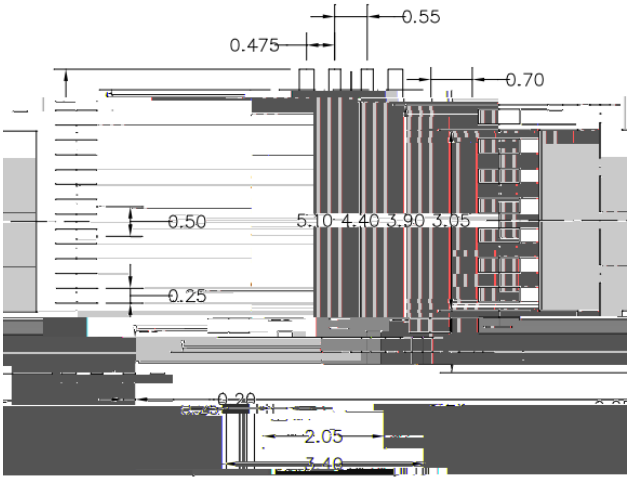


PACKAGE INFORMATION







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