36V Vin Quad Channels Automotive PMIC

FEATURES

- 1 x Synchronous LV Buck Converters VOUT2, VOUT3:
  - Up to 2A Continuous Output Current
  - Output Voltage Range 0.8V to 2.35V with 50mV Steps
- FCCM/PFM Selectable
- Programmable Power Sequencer for VOUT2, VOUT3 and VOUT4
- RESETB Output for System Management
- External Clock Synchronization
- Simple/QA Watchdog
- Integrated Protection Features:
  - Hiccup Over Current Protection
  - Output Over-voltage/Under-voltage Protection
  - Adjustable Input Voltage Under-voltage Lockout
  - Thermal Shutdown Protection
- Up to 1MHz I2C Interface with Optional Packet Error-Checking (PEC)
- Available in QFN-24 (4mm*4mm)

DESCRIPTION

The SCT61441Q device is a wide input power management IC with four channels output. The device is designed for automotive camera module.

The SCT61441Q integrates one 3A HV Buck, two identical 2A LV Buck and a 400mA LDO. Each channel output is continuously monitored, any over-voltage/under-voltage fault will be detected and the device will enter RESET state. All output voltages are pre-programmed, which saves external feedback divider and minimizes system solution. The switching frequency of HV Buck is 2.1MHz/400kHz selectable. The switching frequency is fixed 2.1MHz for LV buck converters The device features Frequency Spread Spectrum (FSS) with programmable jittering span of the switching frequency and modulation frequency to reduce the conducted EMI.

The device also integrates simple watchdog mode and QA watchdog mode. The dedicated WDI pin allows trigger pulse generated by MCU. Programmable watchdog window is suitable for a wide variety of applications. The RESETB output can be the sequencer of MCU to protect it from device fault.

The SCT61441Q device has protection features such as thermal shutdown, short-circuit protection and over-voltage protection. Disabling all outputs via I2C can reduce the quiescent current to 0.85 mA.

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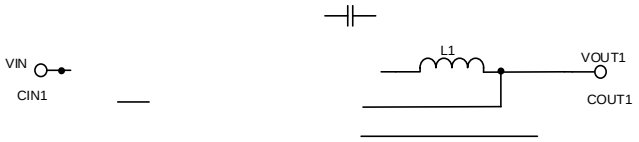
TYPICAL APPLICATION



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RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3.5	36	V
V_{OUT2}	LV Buck2 output voltage range	0.8	2.35	V
V_{OUT3}	LV Buck3 output voltage range	0.8	2.35	V
V_{OUT4}	LDO output voltage range	1.8	3.3	V
T_J	Operating junction temperature	-40	150	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per AEC-Q100-002	-2	+2	kV
	Charged Device Model(CDM), per AEC-Q100-011	-1	+1	kV

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	FCTQFN-24	UNIT
$R_{\theta JT}$	Junction to ambient thermal resistance(1)	39.68	°C/W

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ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMSYMS (23Tc 0A)19.002R(29 0A)31.0020 Tw 14.6E-9.5.4 (RER 8.04 -0 0 .084/P <</MCID26061BDC /TT1 1 Tf -0.004

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ELECTRICAL CHARACTERISTICS

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ELECTRICAL CHARACTERISTICS (continued)

V_{IN}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{OVTH}	Output over-voltage threshold for all outputs	PG1/2/3/4_SEL[1:0]=01, VOUT rising		106		%
		Hysteresis		0]11.7 (EL)]TJ ET528-8 648.24 120.12 23.04 re		

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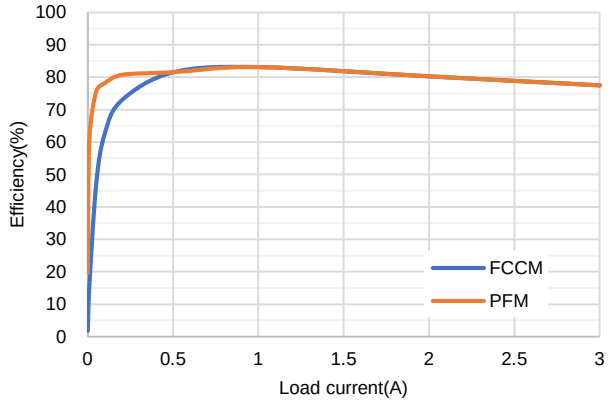
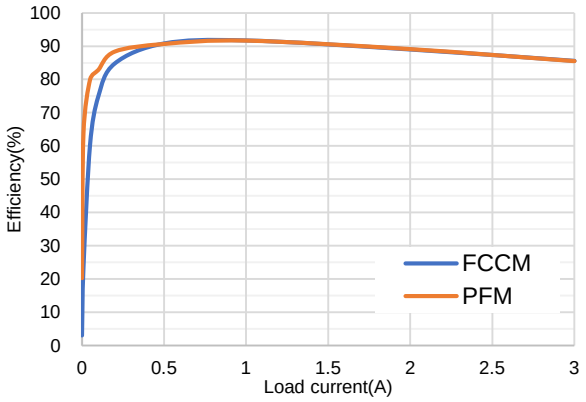
TYPICAL CHARACTERISTICS

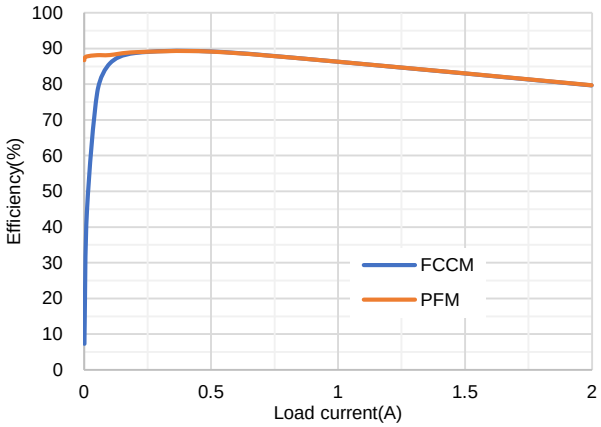
V_{IN}=12V, T_J=-40°C~125°C, unless otherwise noted.



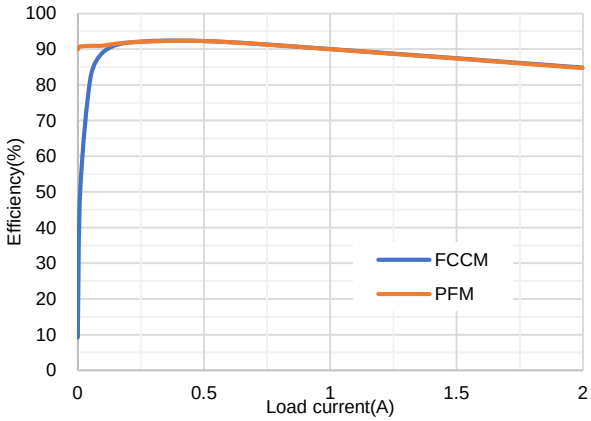
Buck1 Efficiency vs Load Current, V_{OUT1}=3.3V, f_{SW1}=2.1MHz



Buck1 Efficiency vs Load Current, V_{OUT1}=3.3V, f_{SW1}=400kHz



Buck2/3 Efficiency vs Load Current, $V_{OUT2/3}$=1.2V



Buck2/3 Efficiency vs Load Current, $V_{OUT2/3}$=1.8V

LDO PSRR, V_{OUT4}=2.8V, I_{OUT4}=10mA

LDO PSRR, V_{OUT4}=2.8V, I_{OUT4}=100mA

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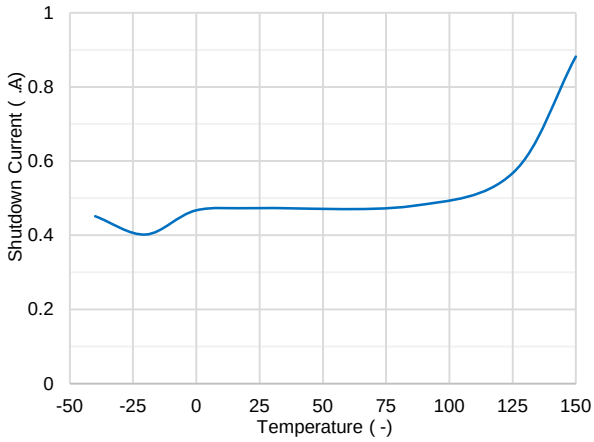
TYPICAL CHARACTERISTICS (continued)

V_{IN}=12V, T_J=-40°C~125°C, unless otherwise noted.



Shutdown Current vs. Temperature

UVLO Rising Threshold vs. Temperature

UVLO Falling Threshold vs. Temperature

VCC vs. Temperature

Buck1 R_{DSON_HS1} vs. Temperature

Buck1 R_{DSON_LS1} vs. Temperature

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TYPICAL CHARACTERISTICS (continued)

V_{IN}=12V, T_J=-40°C~125°C, unless otherwise noted.

Buck2 R_{DSON_HS2} vs. Temperature

Buck2 R_{DSON_LS2} vs. Temperature

Buck3 R_{DSON_HS3} vs. Temperature

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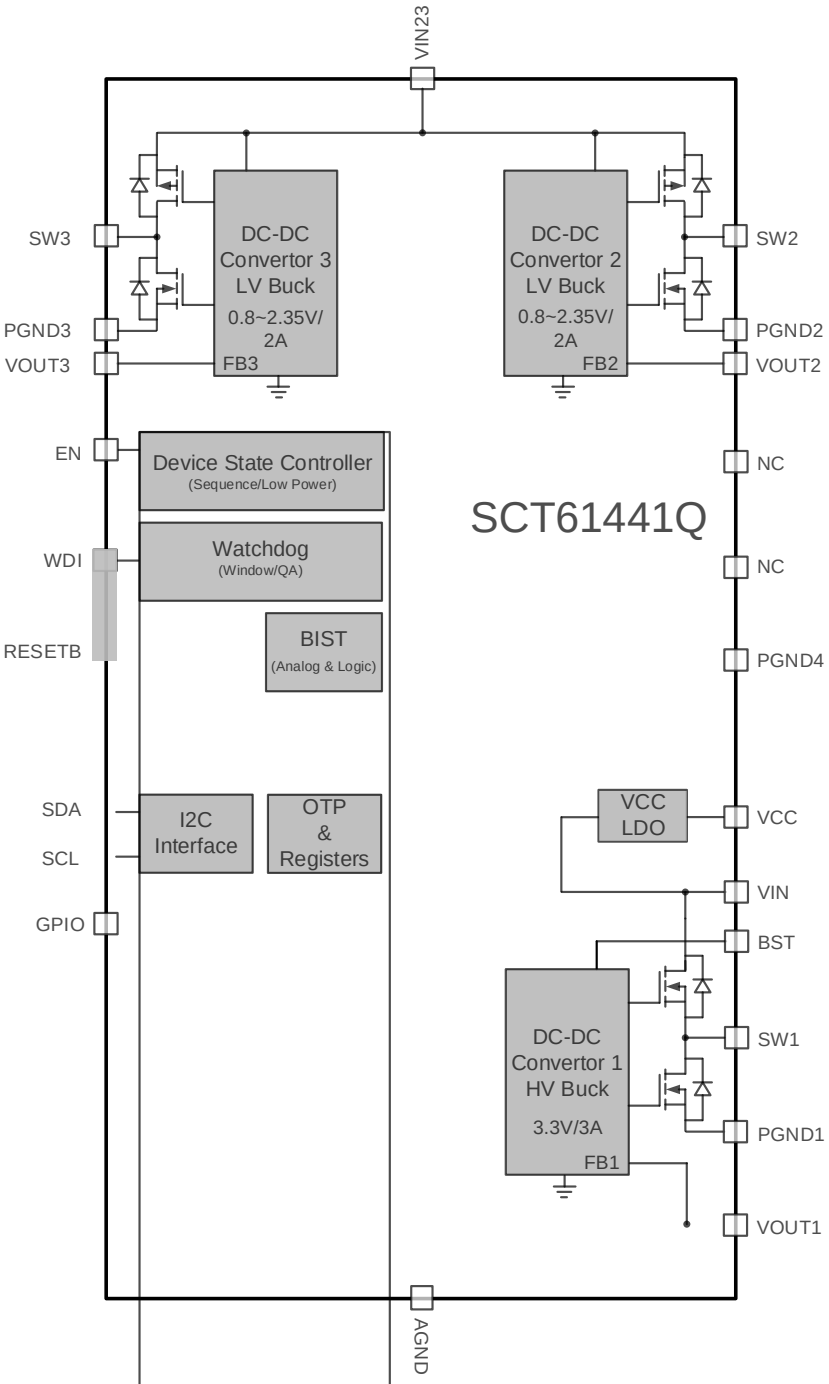
FUNCTIONAL BLOCK DIAGRAM



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OPERATION

Overview

The SCT61441Q device is a wide input power management IC with quad channels output. The device is designed for camera modules in automotive ADAS vision and DMS/OMS applications. The SCT61441Q integrates one 3A HV Buck, two identical 2A LV Buck and a 400mA LV Low-Drop Regulator(LDO). Each channel output is continuously monitored, any over-voltage/under-voltage fault will trigger RESETB pull low. Any deep over-voltage/under-voltage will be detected and the device will enter DEEPSAFE state. All output voltages are pre-programmed, which saves external feedback divider and minimizes system solution. The switching frequency of HV Buck is 2.1MHz/400kHz selectable. The switching frequency is fixed 2.1MHz for LV buck converters. The device features Frequency Spread Spectrum (FSS) with programmable jittering span of the switching frequency and modula Td [(w)son frequency to reduce the conducted EMI.

The devce also integrates sime watchdog mode and QA watchdog mode. The dedicated WDI pin allows trigger pulse generated by MCU. Programme watchdog window is suitable for a wide variety of applscations. The RESETB output can be the sequencer of MCU to protect it from devce fault.

The SCT61441Q devce has protection features such as therm shutdown, short -circuit protection and over-voltage/under-voltage protection. Disabling l outputs v ia I2C can reduce the quiescent current to 0.85 mA.

Operting State Machine

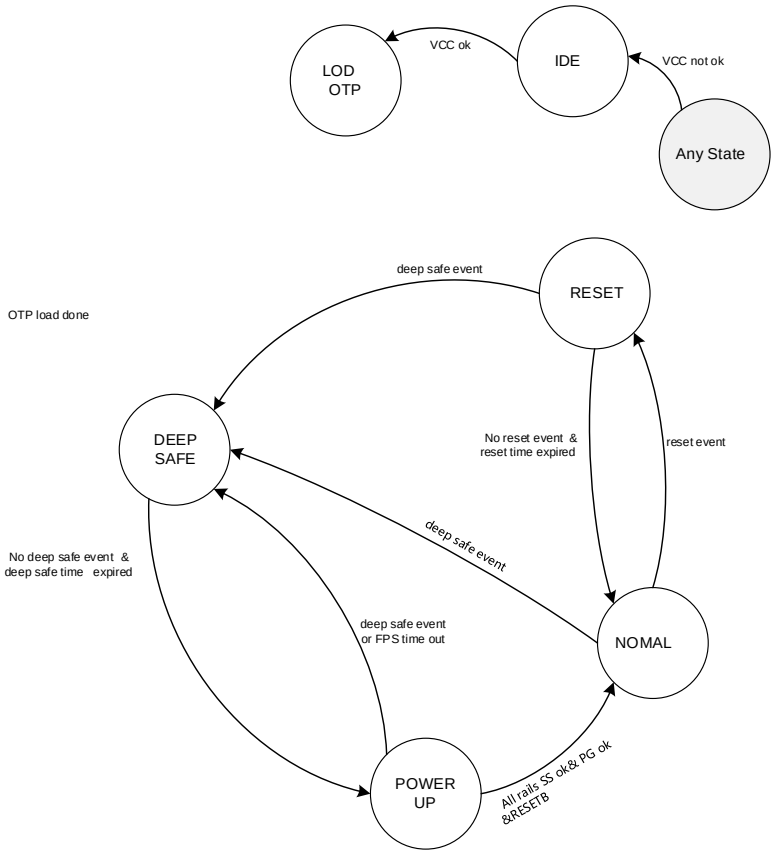

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Table 1. State and Function Matrix Table

State	Function										
	I2C	OTP load	Register reset	HV BUCK1	LV BUCK2	LV BUCK3	LDO4	Watchdog	OCP	DOVP/DUVP detect	TSD
IDLE	OFF										

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delay time respectively. The turn on delay time for each is independent and can be adjusted via changing register **CONFIG_PU1** and **CONFIG_PU2**, thus flexible sequence is available. Deep OV/UV protection is activated to protect channels from destructive OV/UV risk. If all channels finish soft-start and they are within power good range, the RESETB rising timer begins. Once the timer is expired, the device will enter NORMAL state and RESETB will output high. If deep safe event occurs, the state will transit to DEEPSAFE state directly.

NORMAL State

The NORMAL state is the normal running of device with all outputs on. The RESETB pin is released after specific delay time upon entering this state. If watchdog is enabled by register **CONFIG_WD3**, watchdog window will start after setting delay time. The delay time is configured by **WD_1UD[2:0]** in register **CONFIG_WD3**. MCU should feed the watchdog via WDI pin or write answer to specified register periodically. When operating in NOMRAL state, the

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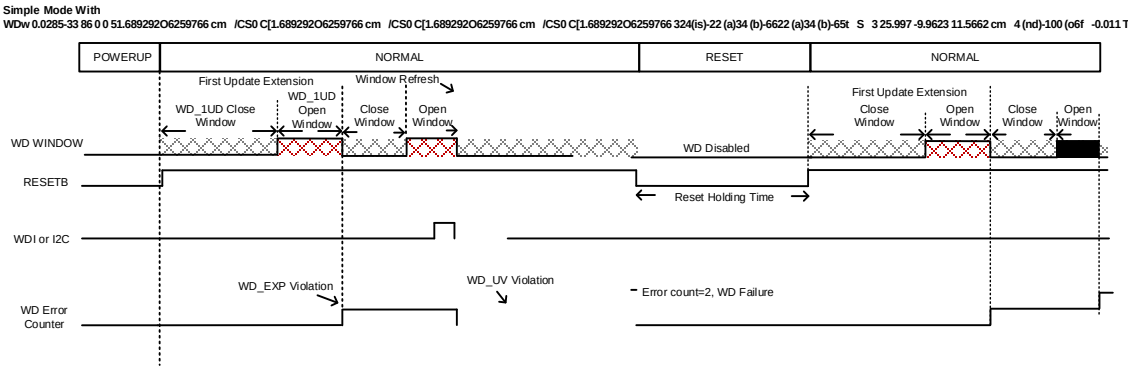

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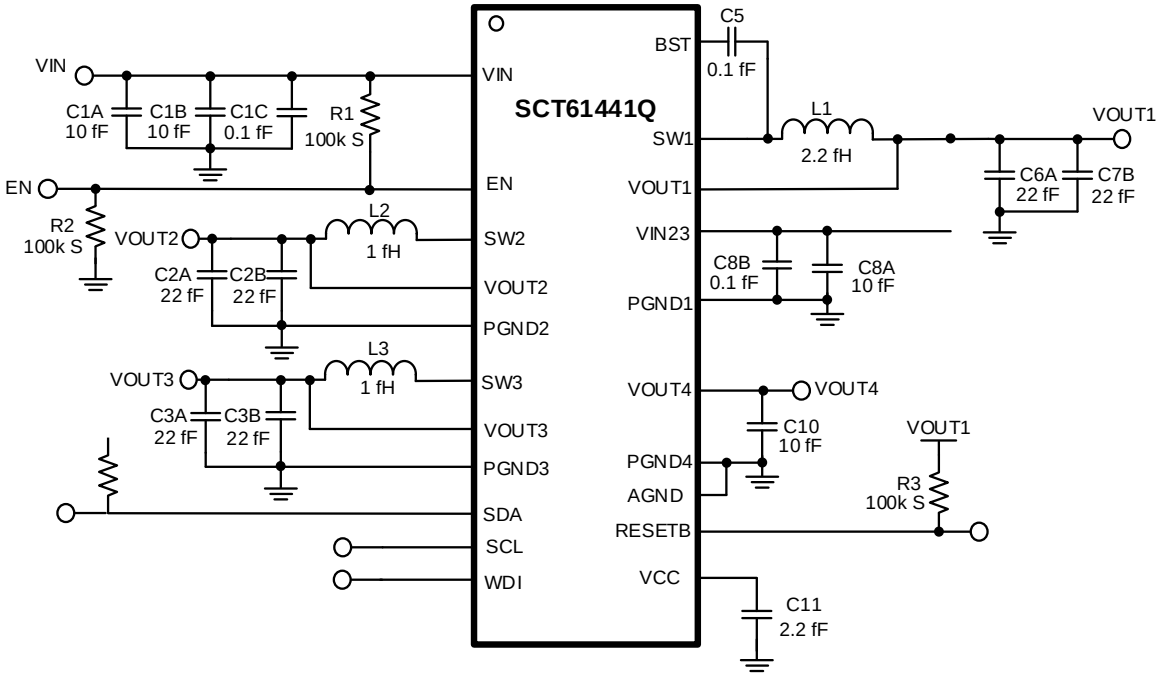
APPLICATION INFORMATION

Typical Application



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Under Voltage Lock-Out

An external voltage divider network of R_1 from the input to EN pin and R_2 from EN pin to the ground can set a higher input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. Use Equation 1 and Equation 2 to calculate the values of R_1 and R_2 resistors.

$$V_{rise} = \left(1 + \frac{R_1}{R_2}\right) \times V_{ENrise} \quad (1)$$

$$V_{fall} = \left(1 + \frac{R_1}{R_2}\right) \times V_{ENfall} \quad (2)$$

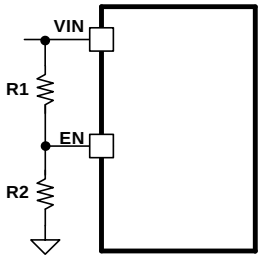

Figure 9. System UVLO by enable divide

where

V_{rise} is rising threshold of Vin UVLO

V_{fall} is falling threshold of Vin UVLO

V_{ENrise} is rising threshold of EN UVLO

V_{ENfall} is falling threshold of EN UVLO

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance(DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20%~40% of the maximum output current.

For a buck converter, the peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 3.

$$I_{LPP\_BUCK} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \quad (3)$$

Where

I_{LPP_BUCK} is the inductor peak-to-peak current of buck

L is the inductance of inductor

f_{SW} is the switching frequency

V_{OUT} is the output voltage

V_{IN} is the input voltage

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 4 to calculate the inductance value.

$$L_{MIN} = \frac{V_{IN(max)}}{I_{OUT(max)} \times 0.4} \times \left(1 - \frac{V_{IN(max)}}{V_{IN}}\right) \quad (4)$$

Where

L_{MIN} is the minimum inductance required

$V_{IN(max)}$ is the maximum input voltage

$I_{OUT(max)}$ is the maximum DC load current

LIR is coefficient of I_{LPP} to I_{OUT}

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Bootstrap Capacitor Selection

$) F H U D P L F F D S D F L W R U P X V W S E H pin Fand QW1 pin for proper operation. A % ceramic

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Layout Guideline

Proper PCB layout is a critical for device's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The rule of thumb is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.

2. Make sure the ground path between VIN capacitor and PGND1 pin is shortest with lowest impendence.

3. Place a low ESR ceramic capacitor as close to VIN1 and VIN23 pin and the ground as possible to reduce parasitic effect.

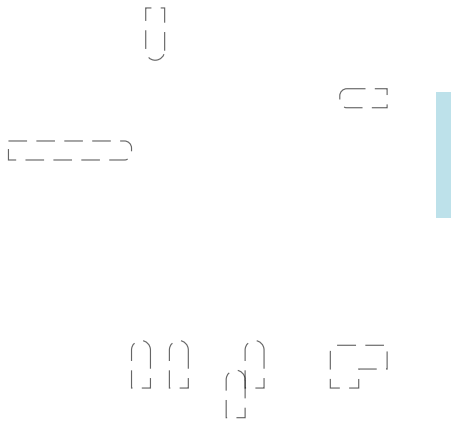
4. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.

5. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias.

6. Output inductor should be placed close to the SW pin. The switching area of the PCB conductor minimized to prevent excessive capacitive coupling.

7. EN UVLO adjust resistors and feedback trace should connect to small signal ground which must return to the GND pin without any interleaving with power ground.

8. For achieving better thermal performance, a four-layer layout is strongly recommended.



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Register Map

ADDRESS	REGISTER	DEFAULT VALUE	OTP ACCESS	I2C LOCK	WD LOCK
0x					

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[7:4]	ON_DELAY3	W/R	OUT3 Power-Up and Recover Turn On delay.	when DELAY_SCALE=00, t_{ON_DELAY3} = ON_DELAY3[3:0] x 0.5ms when DELAY_SCALE=01, t_{ON_DELAY3} = ON_DELAY3[3:0] x 1ms when DELAY_SCALE=10, t_{ON_DELAY3} = ON_DELAY3[3:0] x 2.5ms when DELAY_SCALE=11, t_{ON_DELAY3} = ON_DELAY3[3:0] x 5ms
[3:0]	ON_DELAY2	W/R	OUT2 Power-Up and Recover Turn On delay.	when DELAY_SCALE=00, t_{ON_DELAY2} = O On dela ET Q q 3lODON_DELAYt (hen D)82. Tw 10.831 0 Td (

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[5]	UV_WAR4	Read Clear	UV warning for OUT4, Digital Filter is not included	0 = OUT4 is above UV threshold before DF 1 = OUT4 is below UV threshold before DF
[4]	RESERVED	R	/	/
[3]	UV_WAR3	Read Clear	UV warning for OUT3, Digital Filter is not included	0 = OUT3 is above UV threshold before DF 1 = OUT3 is below UV threshold before DF
[2]	UV_WAR2	Read Clear	UV warning for OUT2, Digital Filter is not included	0 = OUT2 is above UV threshold before DF 1 = OUT2 is below UV threshold before DF
[1]	UV_WAR1	Read Clear	UV warning for OUT1, Digital Filter is not included	0 = OUT1 is above UV threshold before DF 1 = OUT1 is below UV threshold before DF
[0]	RESERVED	R	/	/

STATOV [7:0]				
ADDRESS: 0x0B				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	OV	Read Clear	OV Comparator Status for all channels with Digital Filter.	0 = All enabled channels are below OV threshold after DF 1 = Any enabled channel is above OV threshold after DF
[6]	RESERVED	R	/	/
[5]	OV_WAR4	Read Clear	OV warning for OUT4, Digital Filter is not included	0 = OUT4 is below OV threshold before DF 1 = OUT4 is above OV threshold before DF
[4]	RESERVED	R	/	/
[3]	OV_WAR3	Read Clear	OV warning for OUT3, Digital Filter is not included	0 = OUT3 is below OV threshold before DF 1 = OUT3 is above OV threshold before DF
[2]	OV_WAR2	Read Clear	OV warning for OUT2, Digital Filter is not included	0 = OUT2 is below OV threshold before DF 1 = OUT2 is above OV threshold before DF
[1]	OV_WAR1	Read Clear	OV warning for OUT1, Digital Filter is not included	0 = OUT1 is below OV threshold before DF 1 = OUT1 is above OV threshold before DF
[0]	RESERVED	R	/	/

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[2]	WD_LFSR	Read Clear	LFSR Write Mismatch. The MCU/SoC did not write the correct value to the WDKEY register.	0 = LFSR key match 1 = LFSR key mismatch since last read
[1]	WD_UV	Read Clear	Watchdog Update Violation. The MCU/SoC wrote to the WDKEY register during the CLOSE window.	0 = No violation detected 1 = Watchdog updated too early
[0]	WD_EXP	Read Clear	Watchdog Open Window Expired. The MCU/SoC did not write to the WDKEY register during the whole window.	0 = Watchdog timer not expired 1 = Watchdog timer expired

VOUT2 [7:0]				
ADDRESS: 0x0F				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:5]	RESERVED	R	/	/
[4:0]	OUT2	W/R	OUTI4.9 (/R)]TJ 0 Tc 0ol 00.1Tc 0 T8 0	

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CONFIG_WD1 [7:0]				
ADDRESS: 0x13				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	WD_MODE	W/R	Simple Windowed Watchdog Enable	0 = QA watchdog enabled 1 = Simple watchdog enabled
[6]	WD_SCALE	W/R	Watchdog Clock Divider Scale	0 = 128us 1 = 128us*64
[5:0]	WD_CLK	W/R	Watchdog Clock Divider	tWDCLK = (WD_CLK[5:0]+1) x WD_SCALE

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[0]	I2C_LOCK	W/R	Lock Protection. If 0 by default, then this bit can be changed through the I2C.	0 = All registers can be written. 1 = Writes are ignored to protected registers.

SYS_STATE [7:0]				
ADDRESS: 0x22				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	OTP_CRC_ERR	R	when OTP CRC has error, this bit=1	0 = pass 1 = fail
[6]	RESERVED	R	/	/
[5]	RESERVED	R	/	/
[4]	RESERVED	R	/	/
[3:0]	SYS_STATE	R	System state machine.	0000 = IDLE, 0010 = DEEPSAFE, 0011 = LOADOTP, 0101 = NORMAL, 0111 = POWERUP, 1101 = RESET, others are reserved

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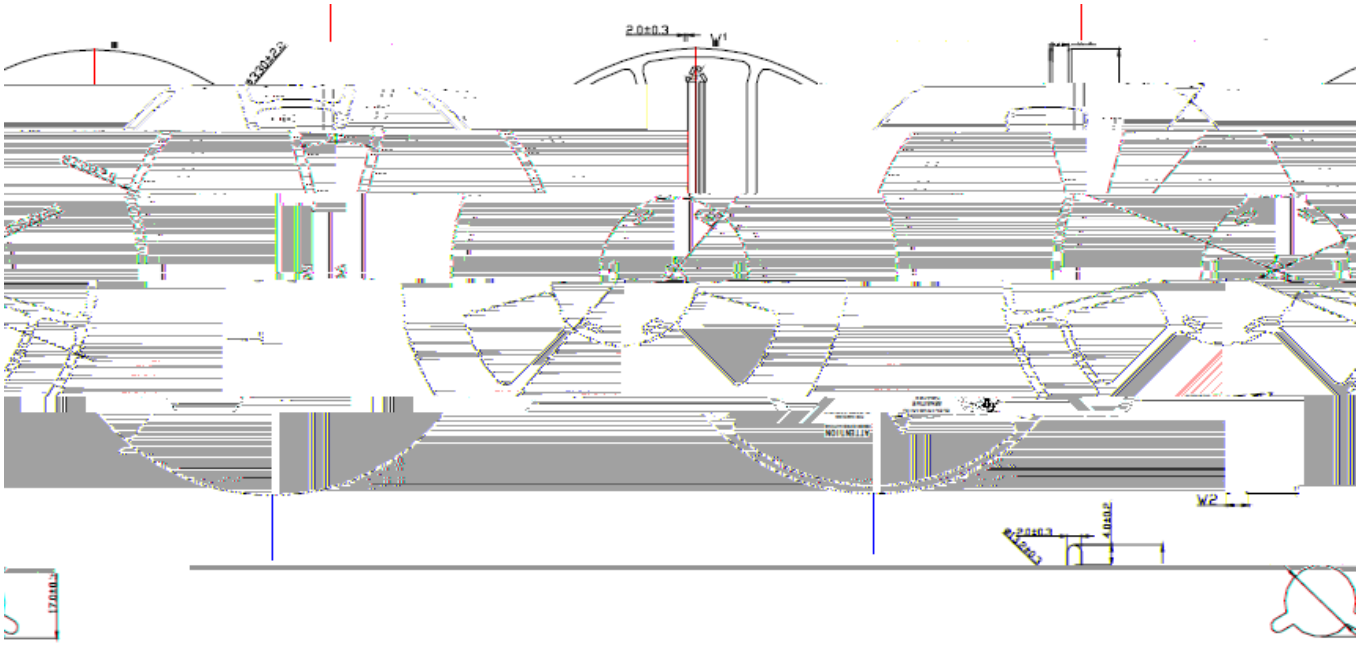
TAPE AND REEL INFORMATION



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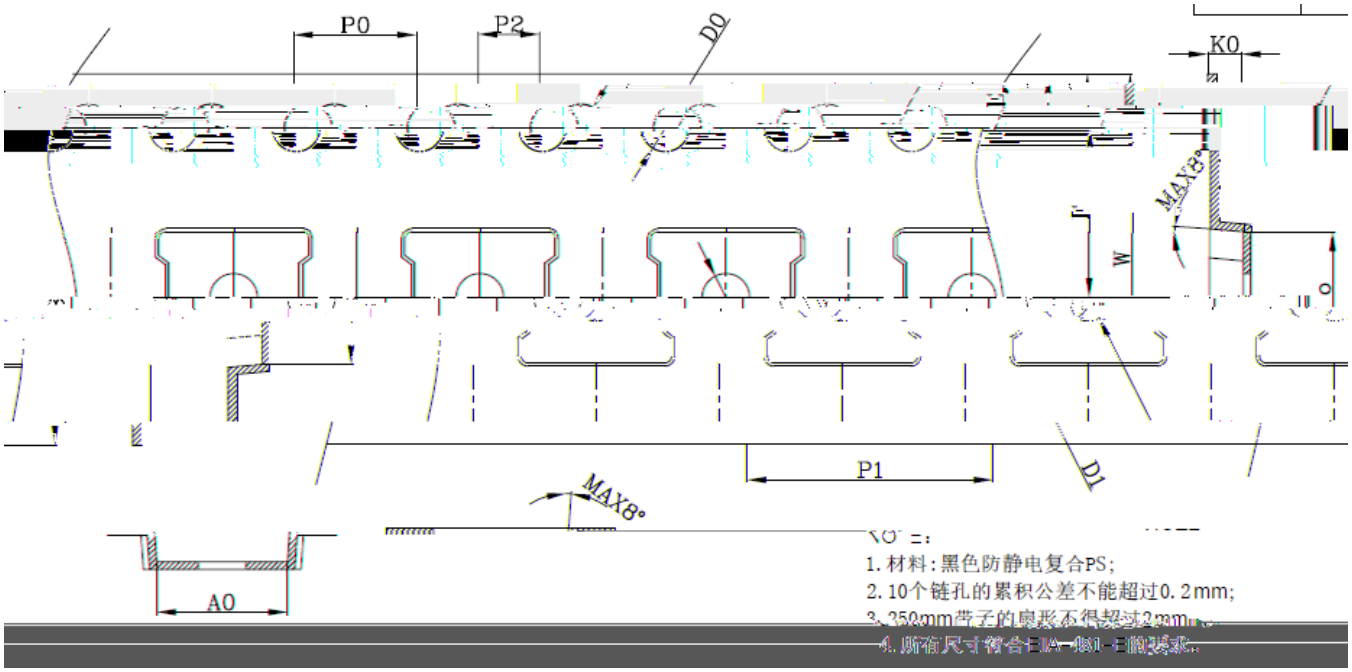

SYMBOL	A0	B0	K0	P0	P1	P2
0.10	8.00±0.10	2.00±0.05	SPEC	4.30±0.10	4.30±0.10	1.10±0.10	4.00±
	D1	W	SYMBOL				
			SPEC				

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